UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,028	03/14/2002	Shinji Furusho	KUBOTA 0007	6569

24203 7590 12/02/2004

GRIFFIN & SZIPL, PC
SUITE PH-1
2300 NINTH STREET, SOUTH
ARLINGTON, VA 22204

EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/088,028	FURUSHO, SHINJI	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2003 and 29 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/13/03, 3/29/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Received

2. Receipt is acknowledged of both sets of information disclosure statement papers submitted on 3/29/02 and 1/13/03, where the papers have been placed of record in the file.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c). In this instance, there are underlines and other marking on the signature page.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it uses legal phraseology such as "comprises". Also, the abstract makes reference to drawings and thus does not allow the reader, regardless of their familiarity with patent documents, to determine the gist of the disclosure with only a cursory inspection since other documents must be also examined. Correction is required. See MPEP § 608.01(b).

6. The title of the invention is not descriptive. Further the title seems to be incomplete or improper. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The scope of the claims is defined by the phrase "The architecture of a parallel computer comprising". Now, it is well known in the art that an architecture of a computer may be drawn out and planned on paper as well as all the modules within it. A computer itself cannot be drawn on paper since it is a tangible entity. The claims do not give a tangible embodiment of an actual computer but instead define an architecture of a computer, which as described above, may be drawn with pencil and paper. To expedite prosecution, the Examiner is interpreting the preamble to read "A parallel computer comprising".

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claims 1 and 9 recite the limitation "the portion" in paragraph 2 of each claim. There is insufficient antecedent basis for this limitation in the claim. A portion of data has not been defined in which the processor manages. The Examiner is taking the claim to mean "a portion."

12. Claim 6 recites the limitation "said bus and memory module" in claim 6. There is insufficient antecedent basis for this limitation in the claim. Multiple buses and memory modules have been defined and it is unclear as to which is being referred. The Examiner is taking the claim to mean "a bus and a memory module" since there are so many of each already defined in an effort to fit the context and give the broadest reasonable interpretation of the claim.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thiel (EP 0 408 810 A1) in view of Hennessy (Computer Organization and Design).

15. In regard to claim 1,

a. Thiel discloses a parallel computer (figure 5) comprising:

i. a CPU module (figure 5, element 56), a plurality of memory modules (figure 5, elements 32a – 32p), each of which having a processor (figure 5, element 48a) and memory core (figure 5, element 50a), and a plurality of sets of buses that make connections between said CPU and memory modules and/or connections among memory modules (figure 5 shows various buses connecting the memory modules (Processors a-p) to each other and to the CPU (control processor), wherein the processors of the various memory modules operate on an instruction given by the CPU to the processors of the various memory, [Column 2, lines 39-42 show that the parallel computer system executes instructions. Column 4, lines 4-6 and figure 5 show that the control processor (CPU) supplies control data (instructions) to the control bus 54 for control of the modules in the system.]

ii. and wherein said architecture of a parallel computer is constituted such that: a series of data having a stipulated relationship is given a space ID and the processor of each memory module manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data, [See column 3, line 4 – column 4, line 1 and figure 8, where the MD Decoder and Address Generator of figure 5 that is within each memory module is illustrated. It is shown that data (having a

relationship of being used by the processor) is uniquely labeled (a space ID) for identification and that the processor in each module detects the data and thus the ID is inherently stored so there is something to compare when detecting. It is also shown that an address of data is decoded and translated for access to main memory and thus stored for use. In addition figure 8 shows several registers (e.g. 140, 142, 112, 114, 118, 120, and 134) that store addresses of data all of which the processor in the memory module manages. Also as shown in that figure and in the text cited above, there are stored upper and lower limits of the addresses and thus a size of the data is known and stored. Since the processor manages all the data it uses, the portion of the series of data is in fact the entire series of data. Further, all the collective storage elements that store this data within the processor or memory module are viewed as a table.]

iii. and the processor of each memory module determines if the portion of the series of data that it manages itself is involved in a received instruction, reads data stored in the RAM core and sends it out on a bus, writes data given via the bus to the RAM core, performs the necessary processing on the data, and/or updates said table. [The Examiner notes that the claim language of this limitation (specifically the placement of the and/or phrase) requires the reference need only show that portion of data managed by the processor performs any of the subsequent functions. As

shown in the section cited above, the processor detects if the data is involved in a read or write and sending the data on the bus.]

b. Thiel does not explicitly disclose the memory modules having a RAM core, but only a local memory.

c. Hennessy has disclosed on pages 16 and 18 the use of RAM memory and that a RAM (random access memory) differentiates from a sequential access memory in that memory access take the same amount of time no matter what portion of the memory is read.

d. Hennessy has then shown on page 541 that RAM (SRAM and DRAM) have a much faster typical access time than a sequential memory such as a magnetic disk. This quick access time would have motivated one of ordinary skill in the art at the time of invention to modify the design of Thiel to use a RAM as the local memory core rather than a sequential access memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Thiel to use a RAM as the local memory core rather than a sequential access memory so that typical memory accesses are faster.

16. In regard to claim 2, Thiel in view of Hennessy discloses the computer architecture according to claim 1, wherein said processor has:

a. a space comparator that compares the space ID given by the CPU against the space ID of one or more series of data that it manages itself, [As shown above the processor compares the data ID to detect it.]

b. an address comparator that compares the logical address given by the CPU against the logical address of the portion of the data that it manages itself, [As shown in the sections cited above, the address is compared with upper and lower limits and thus a comparator exists.]

c. and an address calculator that calculates the physical address in its own RAM cell based on said logical address. [Figure 8 shows that the memory address generator is separate from the other circuitry and thus has its own RAM cell.]

17. In regard to claim 3,

a. Thiel in view of Hennessy discloses the computer architecture according to claim 1,

b. Thiel does not explicitly disclose wherein each of said memory modules receives a synchronization signal for achieving synchronization with the CPU module and other memory modules, and it is constituted such that it comprises input that is connectable to any of said plurality of sets of buses, and output that is connectable to any other of said plurality of sets of buses, and at least, it is able to output data according to said synchronization signal by connecting the input to one of said buses, inputting data and connecting the output to any of said other buses.

c. Hennessy has taught on page 713 synchronizing multiple processors that share the same data from a shared memory (such as the memory modules or processors of figure 5 in Thiel, all of which share bulk or main memory 44). This

is done with some sort of synchronization signal such as a lock over a bus that connects each processor.

d. Hennessy has taught on this same page that synchronization disallows other processors to work on data before another is finished and thus data integrity and correct results are maintained. This integrity would have motivated one of ordinary skill in the art at the time of invention to modify the design of Thiel in view of Hennessy to use synchronization for the multiple processors or memory modules as further taught by Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Thiel in view of Hennessy to use synchronization for the multiple processors or memory modules as further taught by Hennessy so that data integrity is realized.

18. In regard to claim 4, Thiel in view of Hennessy discloses the computer architecture according to claim 3, wherein switches are provided on each of said sets of buses, thereby controlling the connections between said CPU module and the input or output of any of the memory modules, and/or between the input and output of one memory module and the output and input of another memory module, and by switching said switches, the exchange of parallel data is achieved in each of said sets of buses. [Column 10, lines 47-50 show that processors (memory modules) are switched out when dormant or faulty and thus switches exist in the buses to control which processors receive data in parallel.]

19. In regard to claim 5, Thiel in view of Hennessy discloses the computer architecture according to claim 4, wherein the output of one memory module is connected to the input of another memory module via a first bus which is one of said plurality of sets of buses, and the output of said other memory module is connected to the input of still another memory module via a second bus which is another one of said plurality of sets of buses, so that the exchange of data over the first bus proceeds in parallel with the exchange of data over the second bus. [Column 9, line 55 – column 10, line 11 show that data is passed to the data bus from each processor and then written to the destination processor and thus the input of a second processor is the output of a first and the input of a third processor is the output of the second. The section further submits that this may all be done in a single pass or in parallel and thus the function is the same the claimed function and thus data bus of Thiel in view of Hennessy must be subdivided into smaller buses via switching to accomplish such.]

20. In regard to claim 6, Thiel in view of Hennessy discloses the computer architecture according to claim 5, wherein the connections between a bus and a memory module are repeated to form multi-stage connections among memory modules. [As shown in figure 5, the connection between the data bus and memory module (processor) 32a is repeated among each module and forms multi-stage (or multi-module where each module is a stage of sorts) connections among the memory modules.]

21. In regard to claim 7, Thiel in view of Hennessy the computer architecture according to claim 1, wherein, when said processor receives an instruction to delete a specific element within a series of data, insert a specific element into said series of data,

or add a specific element to the end of a series of data, said processor performs a table lookup, compares the region of data that it manages itself against the position of said element subject to deletion, insertion or addition, and based on the results of said comparison, updates the content of said table. [As shown above and in column 3, data is detected by the processor against stored unique labels or ID's for reading data in (insert or addition). This detection is inherently done with a comparator as cited above and the label is stored for future write commands to the bus.]

22. In regard to claim 8, Thiel in view of Hennessy discloses the computer architecture according to claim 1, wherein, in response to a given instruction, said processor converts subscripts for specifying elements within a series of data, and/or executes value conversion for giving a specific modification to elements. [As shown above, the memory module or processor is responsive to instructions. Column 3 further shows how address values or elements are converted to a linear address.]

23. In regard to claim 9,

a. Thiell discloses an information processing unit (figure 5) comprising:

i. a CPU module (figure 5, element 56), a plurality of memory modules (figure 5, elements 32a – 32p), each of which having a processor (figure 5, element 48a) and memory core (figure 5, element 50a), and a plurality of sets of buses that make connections between said CPU and memory modules and/or connections among memory modules (figure 5 shows various buses connecting the memory modules (Processors a-p) to each other and to the CPU (control processor), wherein the processors of

the various memory modules operate on an instruction given by the CPU to the processors of the various memory, [Column 2, lines 39-42 show that the parallel computer system executes instructions. Column 4, lines 4-6 and figure 5 show that the control processor (CPU) supplies control data (instructions) to the control bus 54 for control of the modules in the system.]

ii. and wherein said information processing unit is constituted such that: a series of data having a stipulated relationship is given a space ID and the processor of cache memory module manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data, [See column 3, line 4 – column 4, line 1 and figure 8, where the MD Decoder and Address Generator of figure 5 that is within each memory module is illustrated. It is shown that data (having a relationship of being used by the processor) is uniquely labeled (a space ID) for identification and that the processor in each module detects the data and thus the ID is inherently stored so there is something to compare when detecting. It is also shown that an address of data is decoded and translated for access to main memory and thus stored for use. In addition figure 8 shows several registers (e.g. 140, 142, 112, 114, 118, 120, and 134) that store addresses of data all of which the processor in the memory module manages. Also as shown in that figure and in the text cited above,

there are stored upper and lower limits of the addresses and thus a size of the data is known and stored. Since the processor manages all the data it uses, the portion of the series of data is in fact the entire series of data. Further, all the collective storage elements that store this data within the processor or memory module are viewed as a table.]

iii. and the processor of each memory module determines if the portion of the series of data that it manages itself is involved in a received instruction, reads data stored in the RAM core and sends it out on a bus, writes data given via the bus to the RAM core, performs the necessary processing on the data, and/or updates said table. [The Examiner notes that the claim language of this limitation (specifically the placement of the and/or phrase) requires the reference need only show that portion of data managed by the processor performs any of the subsequent functions. As shown in the section cited above, the processor detects if the data is involved in a read or write and sending the data on the bus.]

b. Thiel does not explicitly disclose the memory modules having a RAM core, but only a local memory.

c. Hennessy has disclosed on pages 16 and 18 the use of RAM memory and that a RAM (random access memory) differentiates from a sequential access memory in that memory access take the same amount of time no matter what portion of the memory is read.

d. Hennessy has then shown on page 541 that RAM (SRAM and DRAM) have a much faster typical access time than a sequential memory such as a magnetic disk. This quick access time would have motivated one of ordinary skill in the art at the time of invention to modify the design of Thiel to use a RAM as the local memory core rather than a sequential access memory.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Thiel to use a RAM as the local memory core rather than a sequential access memory so that typical memory accesses are faster.

24. In regard to claim 10, Thiel in view of Hennessy discloses the information processing unit according to claim 9, wherein said CPU module is constituted such that it can be linked to another bus that connects legacy memory, input devices and display devices to each other. [As shown above, the CPU module controls all system function and thus if the devices of the claim are connected the module will control these devices as well. Examiner notes that the word "can" broadens the scope of the claim so that such a connection is not required, but only capable of performing such a function.]

25. In regard to claim 11, Thiel in view of Hennessy discloses a computer system comprising the information processing unit according to claim 9 and one or more storage devices including legacy memory, input devices and display devices linked to the CPU module via another bus. [Column 11, lines 30-36 shows that the system performs image processing and computer graphics processing and is thus connected to a display device of sorts on another bus.]

Conclusion

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
November 24, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

26. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patent further show the art with respect to distributed systems in general.

US Pat No 5,829,041 to Okamoto teaches a distributed system that has a table for storing a chapter ID, address, and size.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.